Performance Analysis of Comparator using Different Design Techniques

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Abstract - As low power circuits are most popular now-a-days increment in scaling which results in incrementing the leakage power in the circuit, so to get rid of these kinds of leakages and to provide a more desirable power efficiency, we are using distinct types of power gating technique. In this paper, we are going to analyse the distinct types of circuits using low power VLSI design techniques and we are going to display the comparison results. By using this technique power is reduced to approximately 40% to that of GDI comparator. The simulations were done using Micro wind Layout Editor & DSCH software.

Index – Comparator, GDI logic, Sleep Technique, Sleep Stack Technique, VLSI.

1 INTRODUCTION

Comparator is eminent to be an extremely basic and useful component of arithmetic units of the digital systems. In such systems, comparison of any two numbers is said to be an essential arithmetic operation that determine whether a number is greater than, equal to, or less than the other number [1]. Subsequently, comparator is utilized for such operations. To compare two numbers, Magnitude comparator is designed, which is a combinational circuit. Let A and B be the two numbers, and lastly determine their comparative magnitudes and by this means relation between the two (equal to, less than, greater than). Fig.1 depicts the basic block diagram of n-bit magnitude comparator. The outcome of comparison is drawn by 3 binary variables that indicate whether A>B, A=B, or A<B. If two n-bit numbers are to be compared, then the circuit will have 2n inputs & 22n entries in the truth table. For 2- Bit numbers there shall be 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers the truth table would comprise of 6-inputs & 64-rows [2]. Figure 1 shows the block diagram of n-bit magnitude comparator.

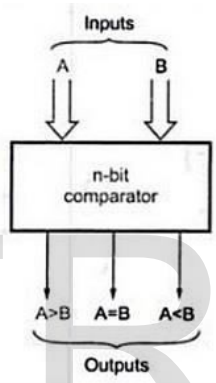


Figure 1: n-Bit Comparator

2 DESIGN APPROACHES

As per latest trends of miniaturization in chip sizes, VLSI design has become a very important research area. In VLSI technology, silicon area, power consumption and propagation delay are the major design issues which play vital role in it.

In today's world, the demand of portable devices is increasing day by day. Thereby, it is required to fabricate more number of devices on a small silicon area to reduce the size of the devices. The main factors on which the portability and reputation of these devices depends are area, number of transistors used to implement basic functionality, power dissipation, speed and reliability.

There are plentiful approaches which will be useful in designing CMOS comparators. Each proposal will put forward different operating speed, power consumption, and circuit complexity. The entire above said criterion may vary evidently from one logic style to another and for that reason legitimate choice of logic style is very important for desirable circuit performance. The main principle of all the design styles and modifications is to bring down the number of transistors to be used to perform the desired logic, lesser the power consumption and attain an increased speed.
Design approach using combinational logic gates helps in designing fastest comparators. Even though increased speed is achieved but at the cost of area which gets increased due to increased transistor count. Power consumption has two main components: Dynamic Power and Leakage power.

Dynamic and leakage power both are the equal involved for the total power consumption. Basically, dynamic power consists of both switching power and short circuit power. As the dynamic power occurs through computing activity, it cannot be completely removed. Static power dissipation results from leakage produced by CMOS transistor parasitic

[2].There are various methods to decrease the power dissipation in VLSI circuits.

The most effective method is to decrease the supply voltage Vdd since CMOS power quadratic ally depends on Vdd. But on the other hand, sub-threshold leakage power increases exponentially [3].

PTL (Pass Transistor Logic) is generally used substitute to CMOS applications and this helps in downsizing transistor count required to carry out logic in certain cases. Another design approach commonly referred to as Gate Diffusion Input (GDI) Logic also helps in decrementing the number of transistors used to implement the logic as compare to CMOS logic style which utilizes both NMOS and PMOS transistors. This technique also helps in decreasing the power consumption.

3 COMPARATOR LOGIC STYLES

The performance here in is concentrated on basic two styles of design which are as under

A. GDI Logic
B. Sleep technique
C. Sleep Stack technique

A. GDI logic

It is also one of the technique which helps in designing low-power digital combinational circuit with fewer number of transistors. Due to devaluation in transistor count, it also allows in reducing power consumption, propagation delay which in turn increases the speed of the circuit, and area of digital circuits while managing low complexity of logic design [4].

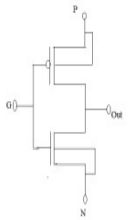


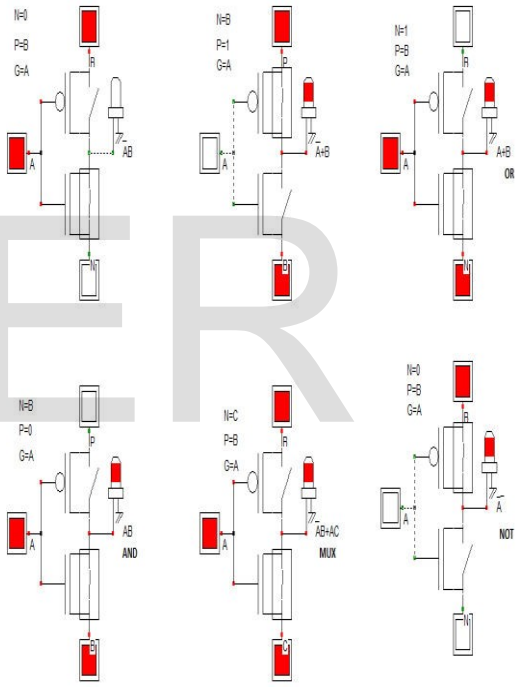
Fig. 2: The Basic GDI cell [4]

Fig.2 shows the basic GDI cell which has three Inputs: G i.e. gate which is common to both NMOS and PMOS, P i.e. input to the source/drain of PMOS and N i.e. input to the source/drain of NMOS. As the GDI cell subsist of only two transistors, so a wide scope of complicated logic functions can be realized using only two transistors. The numerous logic functions which can be implemented by utilizing this basic GDI cell are given in Table 1. All these functions which are described in table can also be implemented using another technique also but GDI technique afford the quick implementation of these functions. This is also best fitted for low power applications.

TABLE 1. LOGIC FUNCTION USING GDI CELL [3]

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

The various functions which can be performed using GDI basic cells are:



B. Sleep Transistor Technique [5]:

In the sleep approach, a "sleep" PMOS transistor is implanted between Vdd and the pull-up network of a circuit and a "sleep" NMOS transistor is located between the pull-down network and ground. These sleep transistors turn off the circuit by disconnecting the power rails. The sleep transistors are turned on when the circuit is active and turned off when the Circuit is idle. By gating the power source, this technique can reduce leakage power effectively.

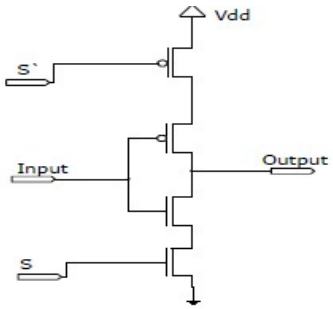


Fig. 3: Sleep method

C. Sleep Stack Technique [8]:

This technique split the individual transistor into two half-size transistors. In this way, every half- transistor is added in series so that there is miniature leakage power.

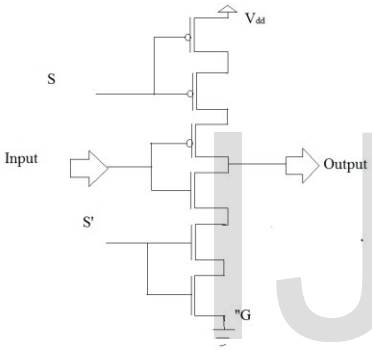


Fig. 4: Stacking technique

It also adds sleepy transistors to disconnect the power supply and ground from the network so that there is no power consumption in off mode.

4 FULL ADDER DESIGNS

Arithmetic unit plays a decisive role in digital electronic devices. Full adder is an elementary block used in arithmetic units. Distinctive logic styles can be used to design the full adder circuit. The main criteria in full adder design are area consumption, speed and power consumption which often clash with the design methodology and act as a constrain on the design of full adder circuits. The XOR gate is the basic building block in full adder circuit. By bettering the performance of the XOR gate, the performance of the full adder can be enhanced. So, there are lot of techniques have been designed to decrease the transistor count and to increase the performance of full adder. These performance criteria's must be individually investigated and analyzed for the efficient performance of the digital circuits.

The full adder module designed by using GDI technique consists of ten transistors to realize the Sum and Carry output. This technique will use in scale down the power consumption. The schematic of this design is shown in Fig.5.

In this circuit, transistorsP1, N1, P2, N2 performs the XNOR operation between A and B inputs. The output of the XNOR block is given to an inverter circuit. Transistors P4, N4, P5, N5 acts as two multiplexers and inverter output will be selection line for these multiplexers. The output of the first multiplexer will result in Sum and output of second multiplexer will result in carry of the full adder.

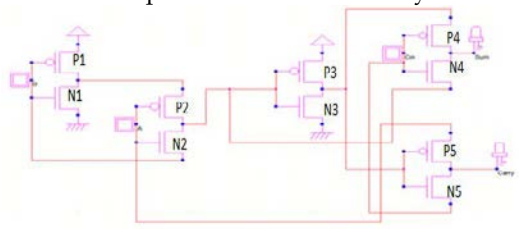


Fig. 5 shows the GDI based full adder

5 PROPOSED 2-BIT COMPARATOR SCHEMATIC

To design the proposed 2-bit comparator, firstly 1-bit full adder has been implemented which utilizes the full adder module which is designed by using GDI approach. The design of proposed comparator based on two techniques i.e., GDI and Sleep Stack. The schematic of 2-bit comparator based on hybridized module is shown in Fig.6

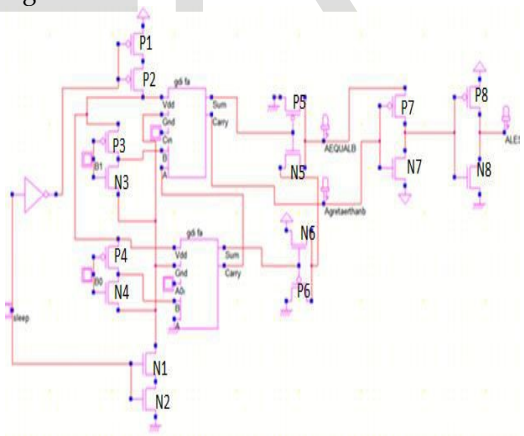


Fig. 6: 2-bit proposed comparator schematic

The 2-bit comparator shown in Fig. 6 is designed to obtain the three outputs after comparing two numbers i.e., to find whether first number is less than, equal to or greater than the third number. This schematic will provide satisfactory performance in terms of area (number of transistors) and power. Furthermore, by applying this 2-bit, a 4-bit comparator can been designed in which carry output of

first 2-bit comparator turn into carry input to the second block of 2-bit comparator. By following the same procedure, 32-bit comparator can be designed. The schematic of proposed 2-bit comparator design is shown in Fig. 6. The proposed comparator is hybridized design because it is designed by using two different logic styles to implement this circuit.

The timing diagram of 2-bit comparator is shown in Fig.7

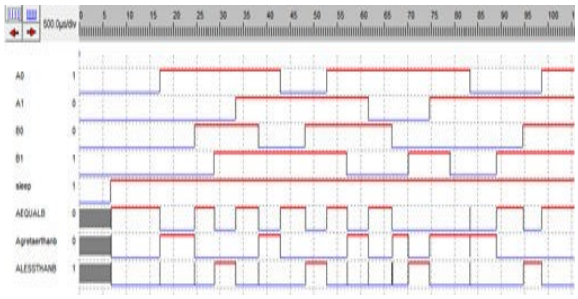


Fig.7 Simulation result of a 2-bit Sleep Stack Comparator

The 2-bit comparator shown in Fig.6 is implemented in DSCH2.7 which consists of two inputs A and B each of having 2-bits. This circuit compares the two numbers and provides three values at the output i.e., A is greater than B, A is less than B or A is equal to B. This comparator utilizes 36 transistors to design the comparator. By using 2-bit comparator, 4-bit can be designed, and then from 4-bit, 8-bit can be designed. Similarly, 16-bit and finally 32-bit comparator can be implemented. The carry output of first 2-bit become input to the second 2-bit comparator block.

6 LAYOUT ANALYSIS

To design the layout of a very complex circuit, it is very difficult to design it manually. So, an efficient and good approach is to use automatic layout generation tool. In this approach, firstly the schematic is designed and validated in DSCH tool at logic level. Then simulation is done to check the functionality of the circuit. Thenceforth verilog file is generated using DSCH which is farther used by MICROWIND tool to generate the layout of the schematic diagram automatically by follow the appropriate design rules. Figure 8 shows the layout of the proposed 2-bit comparator at 120-nm technology. By varying the technology, the area of the layout will also vary.

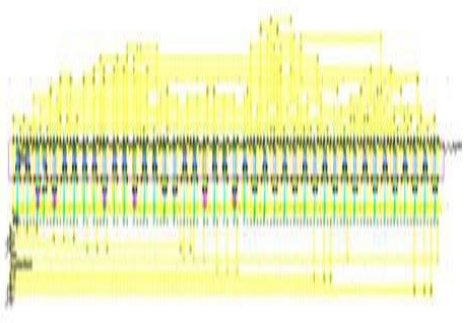


Fig. 8: Layout of proposed 2-bit comparator

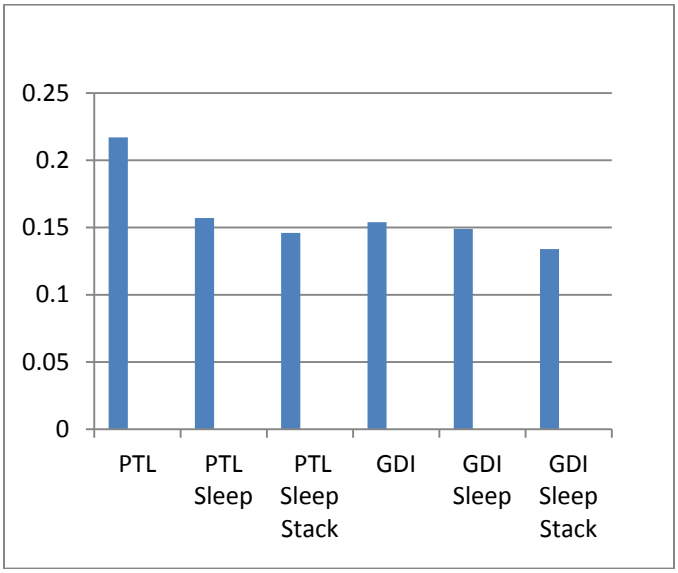
7 RESULTS AND ANALYSIS

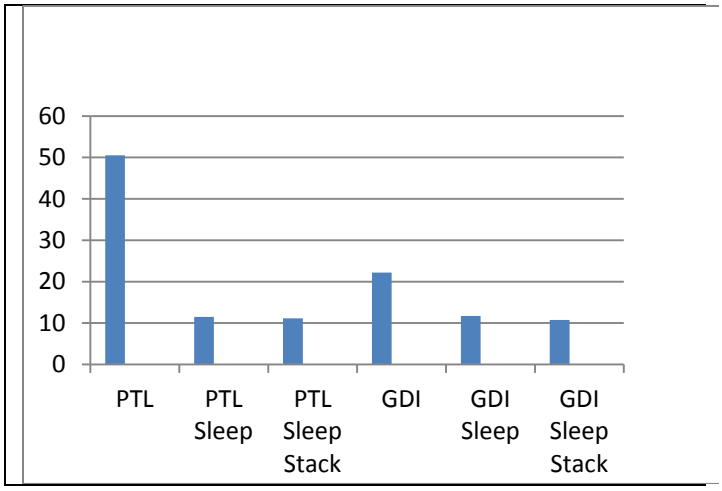
The performance of above specified diverse logic styles based 2-bit comparator has been check out in terms of leakage power and area on 120 nm CMOS technology by using BSIM Level-4 model. Simulation of various schematics drawn in DSCH-2.7 has been done in Microwind2.7f.

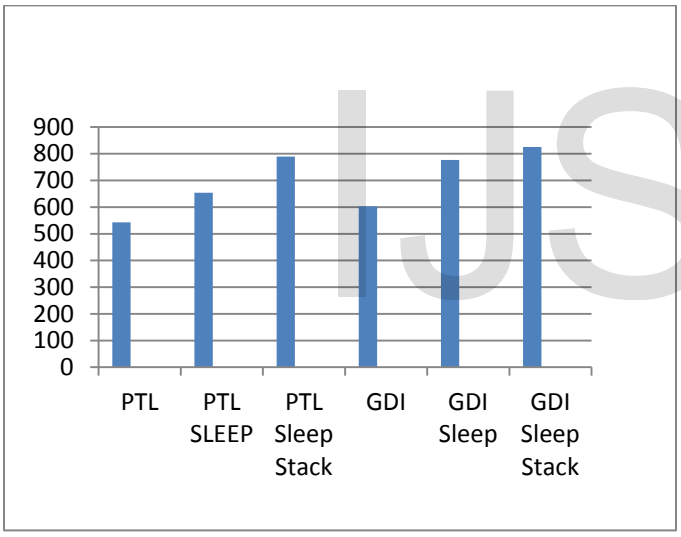
THE RESULTS OF SIMULATION ARE SHOWN IN TABLE 2

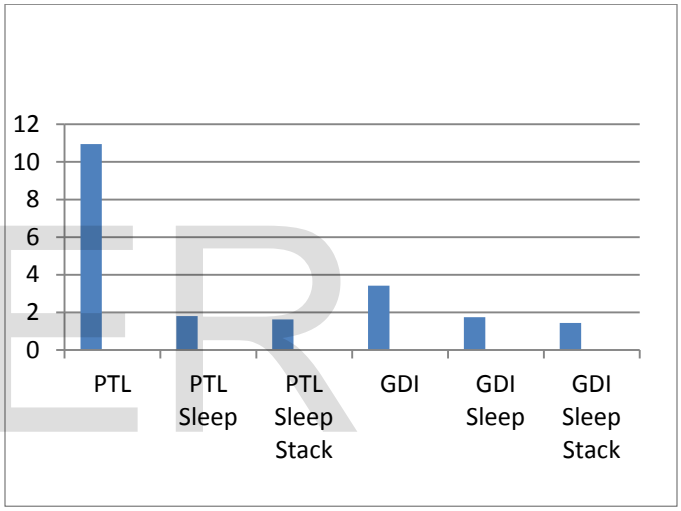
	PTL	PTL SLEEP	PTL SLEEP STACK	GDI	GDI SLEEP	GDI SLEEP STACK
POWER (μW)	0.217	0.157	0.146	0.154	0.149	0.134
SURFACE AREA (μm2)	542.8	653.6	789.6	602.6	776.9	825.3
DELAY (ps)	50.5	11.5	11.135	22.2	11.7	10.75
POWER DELAY PRODUCT	10.95	1.805	1.625	3.418	1.743	1.440

The below graph shows the power consumption of PTL Comparator, GDI Comparator and GDI Sleep Stack Comparator.









8 CONCLUSION

Leakage power consumption is a huge challenge in nanometer scale CMOS technology albeit previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. The proposed technique achieving leakage power consumption with much less speed, especially it shows nearly 40% of power than the existing.

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